# SEMICONDUCTOR DEVICE WITH MOS TRANSISTORS WITH AN ETCH-STOP LAYER HAVING AN IMPROVED RESIDUAL STRESS LEVEL AND METHOD FOR FABRICATING SUCH A SEMICONDUCTOR DEVICE

## Field of the Invention

**[0001]** The present invention relates in general to a semiconductor device with MOS transistors.

## Background of the Invention

**[0002]** Conventionally, MOS transistors are formed in an active zone of a semiconductor substrate that is isolated from the rest of the substrate by an insulation region. The insulation region may be, for example, a region of the type with shallow trenches (STI: shallow trench isolation). Source and drain regions are formed which delimit a channel between them, and a gate region is formed above the channel. All of this is covered with a dielectric layer in which contact holes are etched for electrical connection of the transistors. An etch-stop layer, for example, a nitride layer without any edges, is between the substrate and the dielectric layer.

**[0003]** Residual stress of the etch-stop layer modifies the performance of the transistor, in particular, the current $I_{ON}$ flowing between the drain and the source in the on-state. This current may be increased or decreased depending on the level of the mechanical constraint applied to the transistors. This is due to the fact that the stop layer induces a local

curvature in the substrate of the semiconductor device, which generates a mechanical constraint in the channel. Such a constraint effects the mobility of the carriers, and therefore the performance of the transistor.

**[0004]** By using these properties, the performance of the transistors can be improved by modifying the residual stress level of the stop layer through the implantation of germanium (Ge) in a stop layer that includes nitride. This can be done since the insertion of ions into the nitride destroys the mechanical constraint applied to the silicon.

**[0005]** An etch-stop layer having a negative residual stress level improves the operation of a PMOS transistor but degrades the operation of an NMOS transistor. Conversely, an etch-stop layer having a positive residual stress level improves the operation of NMOS transistors but degrades that of PMOS transistors. Hence, any improvement made to one type of transistor is obtained at the detriment of the other type of transistor. Consequently, ion implantation in the nitride makes it possible either to improve the operation of PMOS transistors or to improve the operation of NMOS transistors, depending on the type of stop layer used.

## Summary of the Invention

**[0006]** In view of the foregoing background, an object of the present invention to provide a semiconductor device having MOS transistors, and a method for fabricating the same, so that the residual stress level of an etch-stop layer is discriminately adapted to the type of transistors that it covers.

**[0007]** This and other objects, advantages and

features in accordance with the present invention are provided by a semiconductor device comprising a semiconductor substrate in which MOS transistors are formed therein, a dielectric layer that covers the substrate and in which contact holes are etched, and an etch-stop layer between the substrate and the dielectric layer.

**[0008]** According to a general characteristic of this semiconductor device, the etch-stop layer may include a first layer of material having a first residual stress level and covers some of the transistors, and a second layer of material having a second residual stress level and covers all of the transistors. The thicknesses of the first and second layers, and the first and second residual stress levels may be selected to obtain variations in operating parameters of the transistors with respect to the transistors covered by the first layer of material. By selecting the material of each layer, as well as the thicknesses, it is possible to locally adapt the overall level of residual stress above each type of transistor to improve the performance of the transistors of each type.

**[0009]** According to another characteristic of this device, the MOS transistors may include NMOS transistors and PMOS transistors. The first and second layers of material may have opposite residual stress levels. In this case, the thicknesses of the first layer and of the second layer, and the residual stress levels of the first layer and of the second layer may be determined to obtain a positive stress level above the NMOS transistors and a negative stress level above the PMOS transistors.

**[0010]** For example, the first layer may have a

negative stress level and covers the PMOS transistors, and the second layer may have a positive stress level. Alternatively, the first layer may have a positive stress level and covers the NMOS transistors, and the second layer may have a negative stress level.

**[0011]** According to another characteristic of the semiconductor device, the zone of the second layer covering the first layer may have a substantially zero residual stress. The overall level of residual stress of the transistors covered by the first and second layers is thus further improved.

**[0012]** Another aspect of the present invention is directed to a method for fabricating a semiconductor device with MOS transistors as defined above. The method comprises forming the transistors in a semiconductor substrate, depositing an etch-stop layer on the transistors, depositing a dielectric layer on the etch-stop layer and etching connection holes in the dielectric layer.

**[0013]** Depositing the etch-stop layer may comprise the deposition of a first layer of material that has a first residual stress level and covers some of the transistors, and the deposition on the first layer of a second layer of material that has a second residual stress level and covers all of the transistors. The thicknesses of the first and second layers, and the first and second residual stress levels may be selected to obtain variations in operating parameters of the transistors with respect to transistors covered by the first layer of material.

**[0014]** According to one embodiment of the method, depositing the first layer may involve depositing the layer on all of the transistors, depositing a mask on a

portion of the transistors, etching the exposed layer and then removing the mask.

**[0015]** According to another characteristic of the method, subsequent to the step of depositing the second layer, a localized treatment of the material of the second layer may be carried out at some of the transistors to locally modify the stress level of the second layer. For example, the treatment of the second layer may be carried out by ion implantation, such as by ion implantation of germanium.

## Brief Description of the Drawings

**[0016]** Other objects, characteristics and advantages of the invention will become apparent on reading the following description, which is provided by way of a non-limiting example and is given with reference to the appended drawings, in which:

**[0017]** Figure 1 is a sectional view of a conventional semiconductor device in accordance with the prior art;

**[0018]** Figure 2 respectively shows curves illustrating variation in the current $I_{ON}$ of NMOS transistors and PMOS transistors as a function of the residual stress level of the etch-stop layer of the transistor in Figure 1;

**[0019]** Figure 3 is a sectional view of a semiconductor device according to the present invention;

**[0020]** Figure 4 illustrates another embodiment of a semiconductor device according to the present invention; and

**[0021]** Figure 5 illustrates a particular embodiment of a method for fabricating a semiconductor device

according to the present invention.

## Detailed Description of the Preferred Embodiments

**[0022]** Figure 1 represents the general structure of a conventional semiconductor device with MOS transistors. In the device, only a partial section thereof in which a transistor is formed has been represented in this figure.

**[0023]** This transistor is formed in an active zone (delimited by an insulating region STI) of a semiconductor substrate 10 by forming source regions S and drain regions D which delimit a channel region 12, and by forming a gate G region associated with spacers E so that the gate extends over the channel 12. All of this is covered with a dielectric layer, for example an oxide layer 14, in which connection holes 16 used for electrical connection of the transistors are etched therethrough, with the interposition of an etch-stop layer 18. Only one contact hole, which is used for connecting the drain D of the transistor, has been represented in this Figure 1 for the sake of clarity.

**[0024]** As indicated above, the layer 18 generates mechanical constraints within the substrate 10, in particular within the region of the substrate 10 forming the channel 12. These constraints lead to a modification of the mobility of the carriers and therefore to a modification (which depends on the residual stress level of the stop layer 18) of the performance of the transistor.

**[0025]** Figure 2 represents the residual stress level of the stop layer 18 along the x-axis, and represents a percentage variation in the current $I_{ON}$ between the source and the drain of the transistor in the on-state

along the y-axis. Moreover, Figure 2 shows that the use of a stop layer having a positive residual stress level is accompanied by an increase in the current $I_{ON}$, with respect to a material having zero stress, for an NMOS transistor (line A), and by a decrease in the current $I_{ON}$ for a PMOS transistor (line B).

**[0026]** Conversely, the use of a material having a negative stress level is accompanied by a decrease in the current $I_{ON}$ for an NMOS transistor (curve A), and by an increase in the current $I_{ON}$ for a PMOS transistor (curve B).

**[0027]** Increasing the stress leads to an improvement in the performance of an NMOS transistor and a decrease in the performance of a PMOS transistor. Conversely, the use of a material having a negative stress level, i.e., a compressive material, is accompanied by a decrease in the performance of an NMOS transistor and an improvement in the performance of a PMOS transistor. The curves represented in Figure 2 depend on the architecture and the dimensions of the transistor in question.

**[0028]** Figure 3 represents the structure of a semiconductor device having a stop layer 18 which makes it possible to obtain good performances with regards to both NMOS transistors and PMOS transistors. Only the transistors and the stop layers have been represented in this figure.

**[0029]** The etch-stop layer 18 includes a first layer I of silicon nitride SiN1 as a stop material that covers some of the transistors, namely the transistors of a first type, and a second layer II of silicon nitride SiN2 covering all of the transistors. In the exemplary embodiment illustrated in Figure 3, the first

layer SiN1 covers the PMOS transistors whereas the layer SiN2 covers the first layer SiN1 as well as the NMOS transistors.

**[0030]** Various techniques may be used for depositing the first and second layers. For example, to deposit the stop layer 18 on the transistors, the first layer SiN1 is deposited on all of the transistors and this layer is etched, so as to leave this layer remaining on only one of the transistor types. The resin layer is then removed and the second layer is deposited on all of the transistors.

**[0031]** The first layer SiN1 has a thickness $e_1$ and a residual stress level $\sigma_1$. The second layer SiN2 has a thickness $e_2$ and a residual stress level $\sigma_2$. The stress levels $\sigma_1$ and $\sigma_2$, as well as the thicknesses $e_1$ and $e_2$, are selected to obtain a negative overall level of residual stress above the PMOS transistors, which can improve the operation of the PMOS transistors.

**[0032]** In this case, specifically, the total stress $\sigma_{tot}$ is determined according to the following formula, on the basis of the total thickness $e_{tot}$ of the stack and the individual stresses and thicknesses of each layer, $\sigma_1$, $e_1$, $\sigma_2$ and $e_2$:

$$\sigma_{tot} \times e_{tot} = \sigma_1 \times e_1 + \sigma_2 \times e_2 \qquad (1)$$

**[0033]** In regards to the PMOS transistors, the overall level of stress is given by the following formula:

$$\sigma_{tot} = (\sigma_1 \times e_1 + \sigma_2 \times e_2)/e_{tot} \qquad (2)$$

In regards to the NMOS transistors, the stress level is equal to $\sigma_2$. By expediently selecting nitrides having opposite stress levels and by optimizing the thicknesses of each layer, an improvement in the performance is obtained for both types of transistor simultaneously.

**[0034]** As an example, an overall residual stress level $\sigma_{tot}$ of -486 MPa, i.e., a stop layer that can improve the operation of the PMOS transistors, is obtained in the example considered in Figure 2 by using materials having the following characteristics: $\sigma_1$ = -1000 MPa; $e_1$ = 650 Å; $\sigma_2$ = +850 MPa and $e_2$ = 250 Å.

**[0035]** In the exemplary embodiment illustrated in Figure 3, the first layer SiN1 covers the PMOS transistors. In one variation, and as shown in Figure 4, it is also possible to provide a first layer SiN1 that covers the NMOS transistors. In this case, the thicknesses and the residual stresses of the first and second layers SiN1 and SiN2 will be selected to obtain, above the NMOS transistors, a stop layer having a positive residual stress overall.

**[0036]** Referring now to Figure 5, and according to another embodiment of the method according to the invention, subsequent to the deposition of the second layer, a localized treatment of the second layer SiN2 is carried out above the first layer. This is done to cancel out the residual stress of the zone of this layer which covers the first layer. To do this, for example, a mask M is formed at the positions of the transistors that are covered only by the second layer, so as to leave exposed those transistors that are covered by the first and second layers. Ion implantation is then carried out, for example by

implantation of germanium Ge, to cancel out the residual stress of the upper layer SiN2.